CLAIMS

1. A semiconductor integrated circuit having a test scan arrangement, comprising:

a plurality of scan chains each having an input end and an output end and being arranged in pairs of a first scan chain and a second scan chain;

a plurality of first terminals and second terminals;

compression logic having a plurality of inputs and at least one output, the plurality of inputs being connected to the output ends of the plurality of scan chains, and the at least one output being connected to at least one compression logic output terminal of the semiconductor integrated circuit for external connection;

the plurality of first terminals each being connected to the input end of the first scan chain of one pair of scan chains for external input connection;

the plurality of second terminals each being selectively connected, in a first state, to the input end of the second scan chain of one of each pair of scan chains for external input connection or, in a second state, to the output end of the second scan chain for external output connection;

the input end of the second scan chain of each pair being selectively connectable in the second state to the output end of the first scan chain of each pair.

2. A semiconductor integrated circuit according to claim 1, further comprising a switch associated with each pair of scan chains for selectively connecting the input end of the second scan chain of each pair to the output end of the first scan chain of each pair, or the input end of the second scan chain of each pair to one of the plurality of second terminals.

3. A semiconductor integrated circuit according to claim 1, further comprising a plurality of multiplexers, each of the plurality of multiplexers being associated with one of the pairs of scan chains, and having a first multiplexer input connected to the output end of the first scan chain of a pair, a second multiplexer input connected to one of the second

terminals for external input connection, and a multiplexer output connected to the input of the second scan chain of each pair.

4. A semiconductor integrated circuit according to claim 1, further comprising a plurality of gates, each gate being connected between the output end of the second scan chain of one of each pair of scan chains and one of the plurality of second terminals to selectively connect, in the second state, the output end of each second scan chain to one of the plurality of second terminals.

5. A semiconductor integrated circuit according to claim 1, further comprising a switching arrangement arranged to selectively connect the output end of the first scan chain of each pair to the input end of the second scan chain of each pair, the input end of the second scan chain of each pair one of the second terminals, and the output end of the second scan chain of each pair to one of the second terminals.

6. A semiconductor integrated circuit according to claim 1, wherein the compression logic is arranged to receive signals from the output ends of the plurality of scan chains and to produce at least one compressed output at the compression logic output terminal.

7. A semiconductor integrated circuit according to claim 6, wherein the compression logic comprises a multiple input shift register.

8. A semiconductor integrated circuit according to claim 6, wherein the compression logic comprises an XOR tree.

9. A semiconductor integrated circuit according to claim 6, wherein the semiconductor integrated circuit comprises a plurality of blocks, and the compression logic comprises an XOR tree arranged on each block each having an XOR tree output, and a further XOR tree arranged to receive the XOR tree outputs.

10. A semiconductor integrated circuit having a test scan arrangement, the arrangement comprising:

a plurality of connected blocks;

plurality of scan chains on each block each having an input end and an output end;

compression logic having a plurality of inputs and at least one output, the plurality of inputs being connected to the output ends of the plurality of scan chains, the at least one output being connected to at least one compression logic output terminal of the semiconductor integrated circuit for external connection;

the compression logic comprising a distributed XOR tree arrangement comprising an XOR tree located on each block and having a block XOR tree output, and a further XOR tree connected to each block XOR tree output and connected to at least one compression logic output terminal of the semiconductor integrated circuit for external connection.